MO-9100A

1-80 MHz High Performance Oscillator

Helping Customers Innovate, Improve & Grow

Features

- Any frequency between 1 and 80 MHz accurate to 6 decimal places
- CMOS compatible output
- Ultra low phase jitter: 0.5 ps (12 kHz to 20 MHz)
- Industrial and extended commercial temperature ranges
- Standard 4-pin packages: 2.5 x 2.0, 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm

Applications

- Computing, storage, networking, telecom, industrial control
- SATA, SAS, Ethernet, PCI Express, video, WiFi

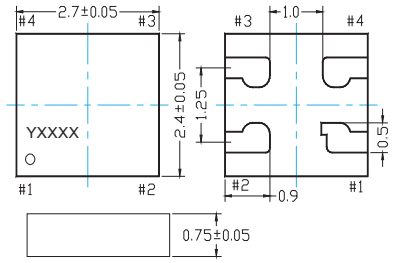
Performance Specifications

Parameter and Conditions	Symbol	Min.	Typ.	Max.	Unit	Condition
Output Frequency Range	f	1	-	80	MHz	
Frequency Stability	F_stab	-10	-	+10	PPM	Inclusive of Initial tolerance at 25 °C, and variations over operating temperature, aging, supply voltage and load
		-50	-	+50	PPM	
First year Aging	F_aging	-1.5	-	+1.5	PPM	25°C
10-year Aging		-5	-	+5	PPM	25°C
Operating Temperature Range	T_use	-20	-	+70	°C	Extended Commercial
		-40	-	+85	°C	Industrial
Supply Voltage	Vdd	1.71	1.8	1.89	V	Supply voltages between 2.5V and 3.3V are supported in increments of 0.1 V. Contact Vectron for guaranteed performance specs for supply voltages not specified in this table.
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.97	3.3	3.63	V	
Current Consumption	Idd	-	31	33	mA	No load condition, f = 20 MHz, Vdd = 2.5V, 2.8V or 3.3V
		-	29	31	mA	No load condition, f = 20 MHz, Vdd = 1.8V
OE Disable Current	I_OD	-	-	31	mA	Vdd = 2.5V, 2.8V or 3.3V, OE = GND, output is Weakly Pulled Down
		-	-	30	mA	Vdd = 1.8 V. OE = GND, output is Weakly Pulled Down
Standby Current	I_std	-	-	70	µA	Vdd = 2.5V, 2.8V or 3.3V, ST = GND, output is Weakly Pulled Down
		-	-	10	µA	Vdd = 1.8 V. ST = GND, output is Weakly Pulled Down
Duty Cycle	DC	45	-	55	%	
Rise/Fall Time	Tr, Tf	-	1.5	2	ns	15 pF load, 10% -90% Vdd
		-	3.6	-	ns	30 pF load, 10% -90% Vdd
		-	4.6	-	ns	45 pF load, 10% -90% Vdd
Output Voltage High	VOH	90%	-	-	Vdd	OH = -7 mA, IOL = 7 mA, (Vdd = 3.3V, 3.0V) IOH = -4 mA, IOL = 4 mA, (Vdd = 2.8V, 2.5V) IOH = -2 mA, IOL = 2 mA, (Vdd = 1.8V)
Output Voltage Low	VOL	-	-	10%	Vdd	
Input Voltage High	VIH	70%	-	-	Vdd	Pin 1, OE or ST
Input Voltage Low	VIL	-	-	30%	Vdd	Pin 1, OE or ST
Input Pull-up Impedance	Z_in	-	100	250	kΩ	
Startup Time	T_start	-	6	10	ms	Measured from the time Vdd reaches its rated minimum value
OE Enable/Disable Time	T_oe	-	-	150	ns	f = 80 MHz, For other frequencies, T_oe = 100 ns + 3 cycles
Resume Time	T_resume	-	6	10	ms	Measured from the time ST pin crosses 50% threshold
RMS Period Jitter	T_jitt	-	1.5	2	ps	f = 75 MHz, Vdd = 2.5V, 2.8V or 3.3V
		-	2	3	ps	f = 75 MHz, Vdd = 1.8V
RMS Phase Jitter (random)	T_phj	-	0.6	1	ps	f = 10 MHz, Integration bandwidth = 12 kHz to 20 MHz

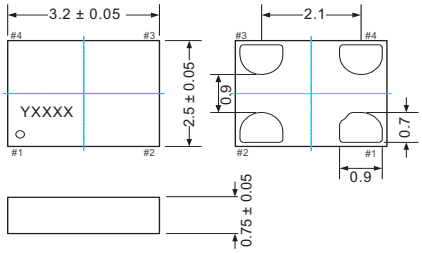
Packaging and Pinout

Package Outline & Dimensions (Unit: mm)

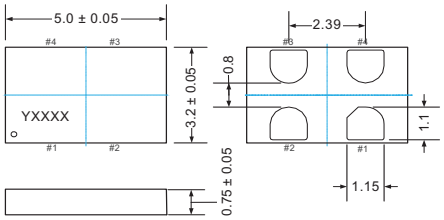
2.7 x 2.4 x 0.75 mm (100% compatible with 2.5 x 2. 0 mm footprint)



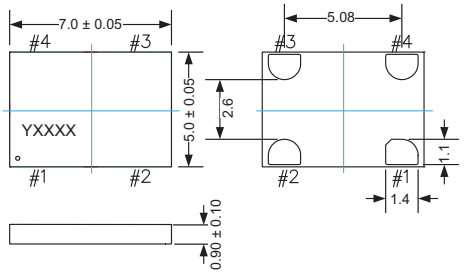
3.2 x 2.5 x 0.75 mm



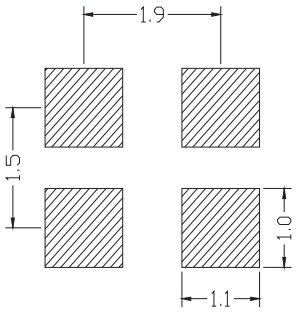
5.0 x 3.2 x 0.75 mm

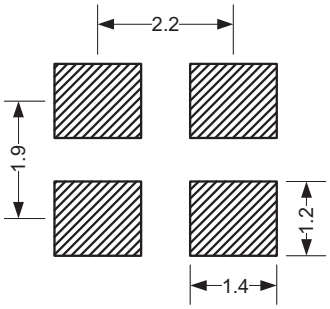


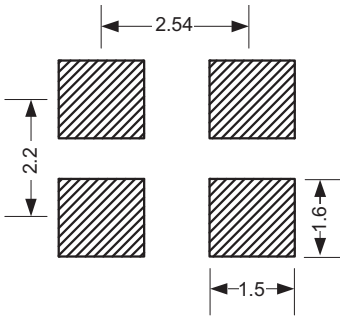
7.0 x 5.0 x 0.90 mm

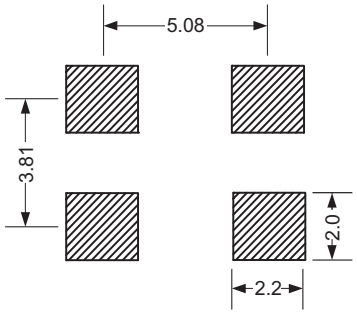


Recommended Land Pattern (Unit: mm)









Pin Connections

Pin	Symbol	Functionality	
1	OE/ ST	Output Enable	H or Open[*]: specified frequency output L: output is high impedance. Only output driver is disabled.
		Standby	H or Open[*]: specified frequency output L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I_std.
2	GND	Power	Electrical and case ground
3	OUT	Output	Oscillator output
4	VDD	Power	Power supply voltage

*A pull-up resistor of <10 kΩ between OE/ ST pin and Vdd is recommended in high noise environment

Top View