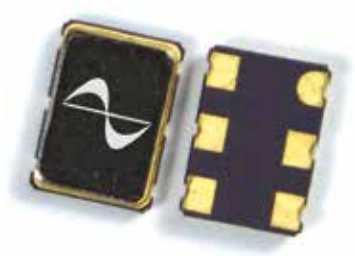
FC7-Series Specifications



7.00L x 5.00W x 1.80H (mm)

Wi2Wi's *FC7-Series* provides precision timing in a hermetically sealed package, and is available in both standard and custom frequencies and configurations. Wi2Wi provides quick-turn sampling for your proto-typing needs, mass production capability, and competitive pricing.

ex) **FC7—T—25000X—C—C—D—3—R—X***

* - for standard or assigned for customization.

ENABLE
T = Tri-State
N = No Connect

FREQUENCY
10000X-99999X = 10.000 MHz – 99.999 MHz
C10000-C99999 = 100.00 MHz – 999.99 MHz
M10000-M15000 = 1000.00 MHz – 1500.00 MHz

OUTPUT
O = LVCMOS
M = LVDS
P = LVPECL

FREQUENCY STABILITY
C = ±50
D = ±100
S = Special

OPERATING TEMPERATURE
A = 0 to +70°C
B = -20 to +70°C
D = -40 to +85°C
S = Special

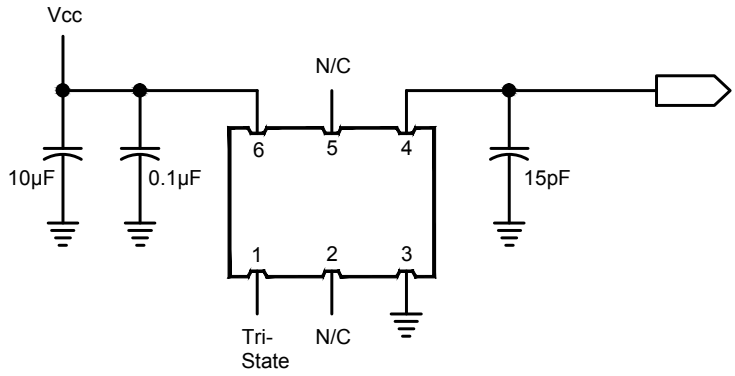
SUPPLY VOLTAGE
2 = 2.5
3 = 3.3

PACKAGE
R = Tape & Reel

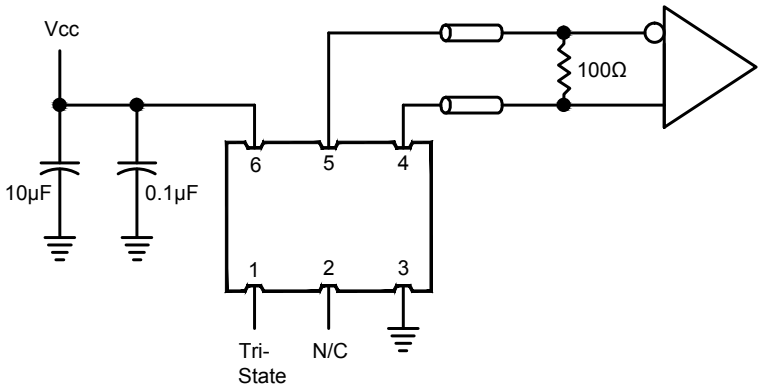
Parameter		Supply Voltage (±10%)		Units
		3.3	2.5	V
Frequency Range	Low (LVCMOS/LVDS/LVPECL)	10.000000		MHz
	High (LVCMOS)	200.000000		
	High (LVDS/LVPECL)	1500.000000		
Frequency Stability	All Causes (Maximum)*1	Per Option		ppm
Temperature Range	Operating	Per Option		°C
	Storage	-55 to +125		°C
Supply Current (Maximum, no Load)	10.000 to 200.000MHz (LVCMOS)	25		mA
	10.000 to 1500.000MHz (LVDS/LVPECL)	65		
Load		See Load/Test Circuits (Page 2)		
Duty Cycle (at 50% Vcc)		45 to 55		%
Rise/Fall Times (Maximum under Load)	10.000 to 200.000MHz (LVCMOS)	3.0		nS
	10.000 to 1500.000MHz (LVDS/LVPECL)	0.6		
Start up Time (Maximum)		15.0		mS
Output Voltage Levels (LVCMOS)	High (Minimum)	90		% Vcc
	Low (Maximum)	10		
Output Voltage Levels (LVDS)	High	1.43 Typ , 1.60 Max		V
	Low	0.90 Min , 1.10 Typ		
	Differential Voltage	250 Min , 350 Typ , 450 Max		mV
Output Voltage Levels (LVPECL)	High	Vcc-1.025 Min , Vcc-0.95 Typ , Vcc-0.88 Max		V
	Low	Vcc-1.810 Min , Vcc-1.70 Typ , Vcc-1.62 Max		
	Differential Voltage	595 Min , 750 Typ , 930 Max		mV
Pin 1 (Tri-State Option Only)	Enable	80		% Vcc
	Tri-State (Disable)	10		% Vcc
Phase Jitter Maximum (rms)	Fractional Divider (12KHz to 20MHz)	1.0		pS
	Integer Divider (12KHz to 20MHz)	0.6		
Period Jitter Maximum (rms)		2.5		pS

*1 - Inclusive of Tolerance @25°C, Operating Temperature, Supply Voltage, Load, 1st Year Aging, Shock and Vibration.

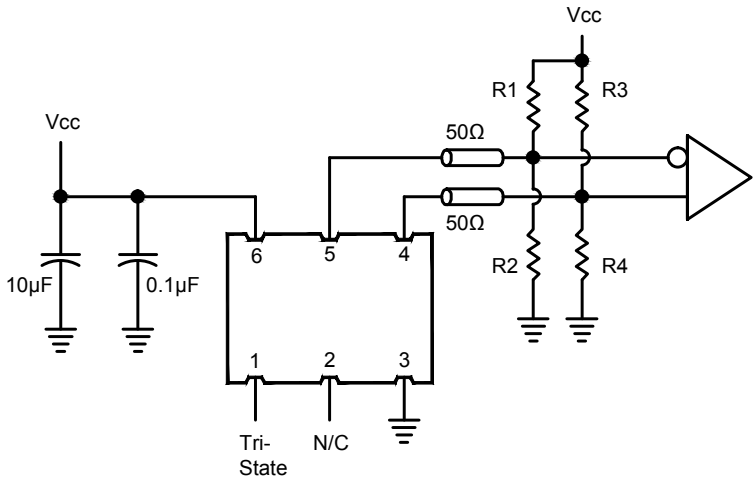
Load/Test Circuits



LVCMOS Test Circuit



LVDS Test Circuit

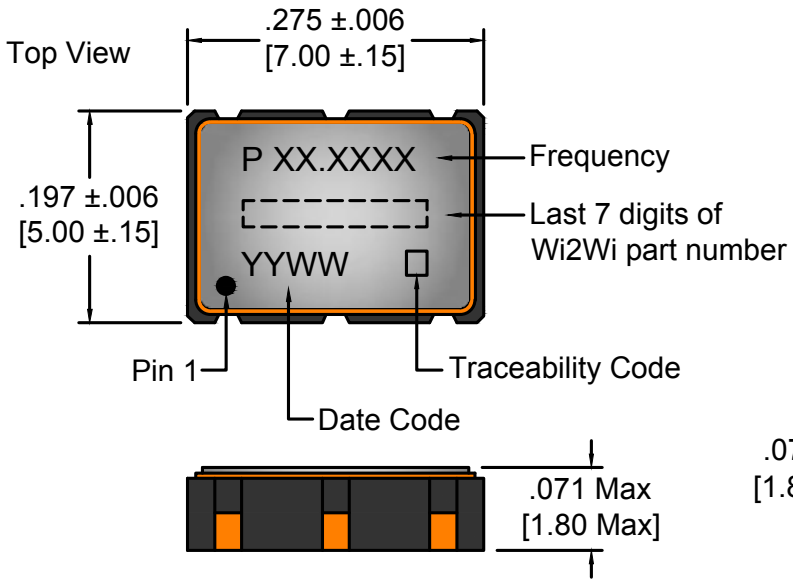


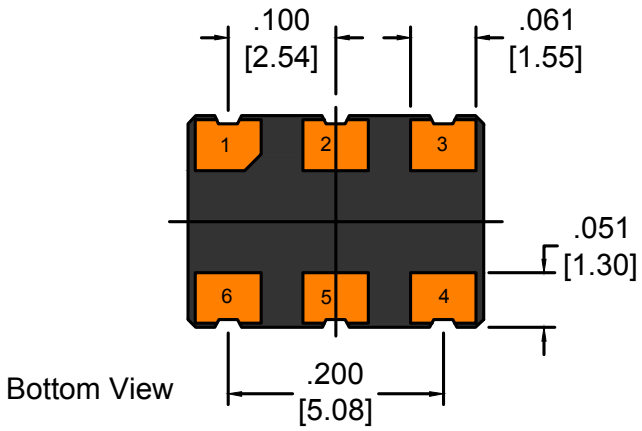
LVPECL Test Circuit

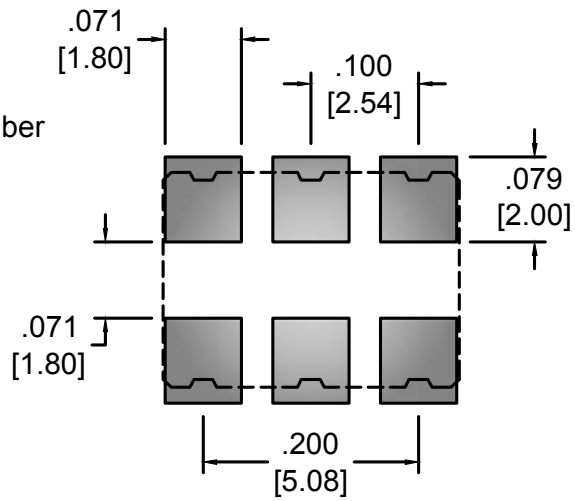
Vcc @ 3.3V: R1/R3 = 127Ω , R2/R4 = 82.5Ω
Vcc @ 2.5V: R1/R3 = 250Ω , R2/R4 = 62.5Ω

PACKAGE DIMENSIONS

Tolerance: ±.008 [.20mm] (Unless otherwise specified)







Recommended Land Pattern
(Top View)

PIN	CONNECTION
1	Tri-State or No Connect
2	No Connect
3	Ground/Case
4	Output
5	Complementary Output (LVDS & LVPECL) No Connect (LVCMOS)
6	Supply Voltage

Contacts: Electro Au, 11.8 to 40.0 µinches (.30 to 1.0 µm) over Electro Ni, 50 to 350 µinches (1.27 to 8.89 µm)

NOTES:

Other options are available, please consult factory.
All product is supplied *RoHS* and *REACH* compliant.
Product can be supplied on Tape and Reel, on reels of 1,000 units.
Specifications subject to change without notice, last updated 3/21/16.

FC7-Series 7.00 x 5.00 x 1.80 (mm)

1. Material: Black Conductive Polystyrene or equivalent.
2. 10 Sprocket Hole pitch cumulative tolerance of ±.008.
3. Camber in compliance with EIA 481.
4. Empty pockets: Trailing end (Minimum) 200 mm. and Leading end (Minimum) 400 mm.
5. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.